ESD-TR-66-399

Technical Note

1966-33

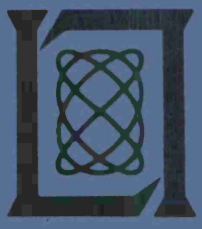
N. L. Daggett

Lincoln Experimental Terminal Timing and Frequency Control

4 August 1966

Prepared under Electronic Systems Division Contract AF 19(628)-5167 by

Lincoln Laboratory
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Lexington, Massachusetts



The work reported in this document was performed at Lincoln Laboratory, a center for research operated by Massachusetts Institute of Technology, with the support of the U.S. Air Force under Contract AF 19(628)-5167.

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LINCOLN EXPERIMENTAL TERMINAL TIMING AND FREQUENCY CONTROL

N. L. DAGGETT

Group 62

TECHNICAL NOTE 1966-33

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LEXINGTON MASSACHUSETTS

ABSTRACT

The Lincoln Experimental Terminal timing and frequency control provides digital control signals to the frequency synthesizers which determine transmit and receive frequencies and system timing signals to such equipment as the sequential encoder-decoder and the sync recovery system. Every 200 μsec a new 15-bit frequency control word is sent to the transmit and receive synthesizers, the transmit word containing the information signal plus one-way doppler prediction superimposed on the frequency-hopped base frequency, and the receive word containing one-way doppler prediction plus measured frequency error superimposed on the base frequency. Every 5 ms a sync signal is substituted for the information signal in the transmit word and a separate frequency control word is sent to the sync receiver frequency synthesizer. Timing of all output signals is variable in response to predicted path delay and measured time error.

Accepted for the Air Force
Franklin C. Hudson
Chief, Lincoln Laboratory Office

LINCOLN EXPERIMENTAL TERMINAL TIMING AND FREQUENCY CONTROL

I. INTRODUCTION

The equipment to be described provides digital control signals to the frequency synthesizers and system timing signals for the Lincoln Experimental Terminal.[1,2] These signals are synchronized with those from other terminals by means of time data from the master clock, path delay and doppler shift corrections from the orbital computer (predicted values), and measured errors from the sync recovery system. Three nearly identical sections (Fig. 1) form the control: the transmit section provides control for outgoing signals, the monitor section provides for reception of the transmitted signal as retransmitted from an active satellite, and the receive section provides control for the reception of signals from another terminal.

Control for the basic frequency-hopping comes from a separate pseudo-random sequence generator in each section (Fig. 2). In the transmitting section, the sequence generator output is summed with the four-bit information symbol from the sequential encoder. (A periodic sync signal is introduced by suppressing the information symbol and transmitting a known fixed symbol.)

II. FUNCTIONAL DESCRIPTION

A. Frequency Control

1. Sequence Generator

Figure 3 shows the 36-bit shift-register pseudo-random sequence generator which controls frequency-hopping in each section. Twelve bits of the sequence generator are read out in parallel every 200 μsec to form the frequency control word; the shift register is then shifted 12 times to form the next word. The sequence

1. P. Rosen and R. V. Wood, "The Lincoln Experimental Terminal," IEEE Annual Communications Convention (June 1965).
2. P. R. Drouilhet, "The Lincoln Experimental Terminal Signal Processing System," (Ibid).

generator will thus operate for over a week if desired without repeating its sequence. Since the sequence generators in individual terminals must be synchronized in order to communicate between them, front-panel switches are provided to allow presetting the sequence generators to any desired state. One bank of octal rotary switches determines the reset value for the transmit and monitor section and a second bank controls the receive section.

2. Restriction of Frequency Range

The 12-bit output of the sequence generator is used to form the most significant end of the 15-bit frequency control word. Since this word is modified to include the information bits (in the transmit section only) and the doppler correction, some provision must be made to ensure that this modification does not overflow the 15-bit word. Furthermore, since an identical constraint must be used at both the transmitting and receiving ends and the receiver does not know precisely what doppler correction is used at the transmitter, the constraint must be applied only to the sequence generator output. The method used places an upper bound on the allowed output from the sequence generator; if this is exceeded the next-to-the-most-significant bit of the output word is forced to zero, forcing the value back into the allowed region. The range of numbers above the boundary is made large enough to allow for the maximum expected excursion of doppler plus information; the predicted doppler from the computer is given a permanent bias to allow for positive or negative doppler corrections. In addition, console-mounted bandwidth control switches permit forcing the first one, two, or three most significant bits in the sequence generator output word to zero, thereby reducing the frequency-hopping bandwidth from the normal 20 MHz to 10, 5, or 2.5 MHz.

3. Frequency Correction

Three components are added to the sequence generator output to form the frequency control word: (a) the binary word representing the information symbol to be transmitted (in the transmit section only); (b) the computer predicted doppler correction; and (c) the measured frequency error (in the monitor and receive sections only).

In the transmit section only, a four-bit information symbol from the sequential encoder is added to bits 5 thru 8 (Fig. 3) of the frequency control word (where bit 1 is the least significant bit corresponding to a frequency change of 625 Hz). A fixed sync symbol is periodically substituted for the information symbol to facilitate time and frequency synchronization at the receiving terminal.

The predicted doppler correction from the orbit computer provides for adding a full 15-bit word to the frequency control word. However, the higher order bits of this word are normally zero except for possible use during reduced-bandwidth operation to position the center frequency of the output spectrum. The 15-bit word is treated as unsigned, with negative corrections eliminated by a fixed bias (equal to the maximum negative doppler) added by the computer at all times. The computer will also include, thru manual intervention at the operating console, a manual frequency correction which can be used, as mentioned above, for adjusting operating center-frequency during reduced-bandwidth operation.

In the monitor and receive sections only, a 10-bit frequency correction developed by the sync recovery system is added to the low order end of the frequency control word. This error is also sent directly to the orbit computer but this path is not used for correction because of the excessive delay that might be introduced into the frequency tracking loop. This correction to the frequency control word is also unsigned, with a further bias added to the computer doppler correction to eliminate the need for negative values. (The hardware is simplified by doing this.)

The frequency control word, with all necessary corrections added to the sequence generator output, is stored at 200 μsec intervals in a 15-bit parallel buffer for output to the frequency synthesizers. The control words to the transmit and receive synthesizers are each stepped thru a second buffer to provide an additional 200 μsec delay. This permits additional buffers in the monitor and in the receive section each to receive the sync frequency control word 300 μsec early to enable the monitor and receive sync receiver frequency synthesizers to be changed before the expected time of arrival of the sync transmission.

B. Timing Generation and Control

1. Operating Modes

Four operating modes are available for terminal operation. Two are high rate modes obtained by transmitting a new four-bit information symbol during each 200 μsec

interval for a rate of 5000 symbols per second. Two are low rate modes transmitting 200 symbols per second. Two teletype channels are transmitted in all modes. The highest rate uses a sequential encoding rate $R = \frac{1}{2}$ to provide 10,000 information bits per second (not all of these are available for useful information transfer, however). In this mode 9600-bits per second are used for Voice Excited Vocoder (VEV) operation. All other modes use a coding rate $R = \frac{1}{4}$, resulting in 5000 information bits per second in the other high rate mode, of which 4800-bits per second are used for Pitch Excited Vocoder (PEV) operation. In one of the low rate modes, the Teletype (CW) mode, transmission continues in the same frequency-hopped manner used for the higher rates but each information symbol is repeated 25 times, with appropriate integration at the receiver outputs. The second low rate mode provides for future operation with a pulsed transmitter; in this case each information symbol is sent once during the 200 μsec transmission burst occurring every five milliseconds. (The sequence generators continue their normal frequency-hopping pattern but are ignored except during the transmission interval.)

During the Teletype (Pulsed) mode, sync symbols are transmitted at 125 ms intervals; during all other modes, the sync signal occurs at 5 ms intervals (that is, every 25 transmission intervals).

Regardless of the operating mode in use, the sequential encoder-decoder groups the transmitted symbols in 1000-symbol blocks. Transmission time for a complete block or frame is 200 ms at the high rates or 5 seconds at the low rates.

2. Timing Counters

Identical timing counter chains in each section are used to derive the necessary control signals for sequence generator stepping and sync and frame timing at each end of the system. Phase of the resultant timing structure can be adjusted to compensate for path delay and permit close synchronization of the transmitting and receiving terminals. In normal operation the timing of the transmit section is advanced with respect to reference time by an amount sufficient to compensate for the up-link path delay and the timing of the monitor and receive sections is adjusted to take care of the down-link delay.

Figure 4 shows the timing counter configuration used in each section. The variable-ratio counter (the V-counter) normally divides by five with each state lasting five microseconds for a total cycle time of 25 μsec. When a time adjustment is made by the time offset control, the counter adds an extra state or skips a state (divides by six or four) as appropriate to retard or advance all subsequent timing.

The next counter in the chain, the D-counter, divides the output of the V-counter by eight to produce the 200 μsec period used for the transmission interval (the length of time a given frequency control word is used to control transmitter output frequency).

Both the V-counter and the D-counter have all of their states decoded to provide flexibility in establishing timing control signals. The output of the D-counter clocks two more counter chains in parallel, one containing four binary divider stages, and the other containing six stages, each dividing by five. By combining outputs from these two counters thru trailing-edge logic, timing signals can be generated which occur at multiples of $2^m \times 5^n$ times the transmitting interval (200 μsec), where m can range from 0 to 4 and n from 0 to 6.

Timing controls for the sync, information symbol, and frame timing are derived in this manner, with rate variations for the different operating modes obtained simply by varying the counter output taps used. Advantages of this particular technique are that it offers flexibility in the timing outputs and, especially important, it permits changing from one operating mode to another without loss of counter synchronization. Control over the relative timing of the principal timing outputs (for sync, information symbol, and frame) is provided by passing the basic timing signals thru four-stage shift registers clocked at 200 μsec intervals. This makes it easy to provide control signals which occur before, during, or after a particular transmitting interval.

3. Timing Reset Control

To establish proper synchronization between two operating terminals the sequence generators and time counters in each must have identical time relationships. To accomplish this reset controls are provided which allow an even-ten-minute-interval signal from the station master clock (accurate to better than one millisecond) to clear all timing counters and reset the sequence generators to any arbitrary states. (Sequence generator settings are normally obtained from a precalculated table showing values for even ten-minute intervals.)

When resetting for operation with the moon a reset table is used which includes a 400 ms time offset to reduce the magnitude of the required path delay corrections from the computer and prevent exceeding an 18-bit word length at maximum ranges. When resetting for local loop operation, a fixed reset value identical for all sections may be used to avoid the necessity of setting the rotary switches.

4. Time Correction

As mentioned earlier, all timing in a given section is retarded by extending the cycle of the V-counter by one state, and advanced by shortening the cycle by one state. Each time the V-counter goes thru an extended or shortened cycle an up-down counter in the time offset control (Fig. 5) counts up or down. This counter is part of a digital servo loop which varies the timing according to a time offset command specifying the offset required at any given time. The contents of the up-down counter are compared with the time offset command during each cycle of the V-counter; any difference causes the appropriate error command to change the cycle of the V-counter and count up or down in the up-downcounter until a null is obtained. The direction of time correction is preset for the particular section: for the transmit section timing is always advanced with respect to reference time by the amount of the offset command, for the monitor and receive sections timing is always retarded.

The time offset command is formed in a manner similar to the frequency control word. An 18-bit predicted path delay is provided by the orbit computer, modified by a fixed bias plus any desired manually inserted bias. In addition, in the monitor and receive sections, a 10-bit measured time error is provided by the sync recovery circuits. The components are added together in a parallel adder to produce the time offset command.

C. Reset and Operating Mode Controls

In addition to the circuits which are repeated in each of the nearly identical sections, there is a single group of circuits which provide for independently resetting and controlling the operating mode for the transmit and monitor sections and for the receive section.

Since the mode control signals are sent over long cables from the control console and since transient changes in operating mode would cause momentary interruption of system sync, these signals are clocked at a low (once per second) rate into buffer flip-flops to minimize the likelihood of erroneous changes in rate due to noise pickup.

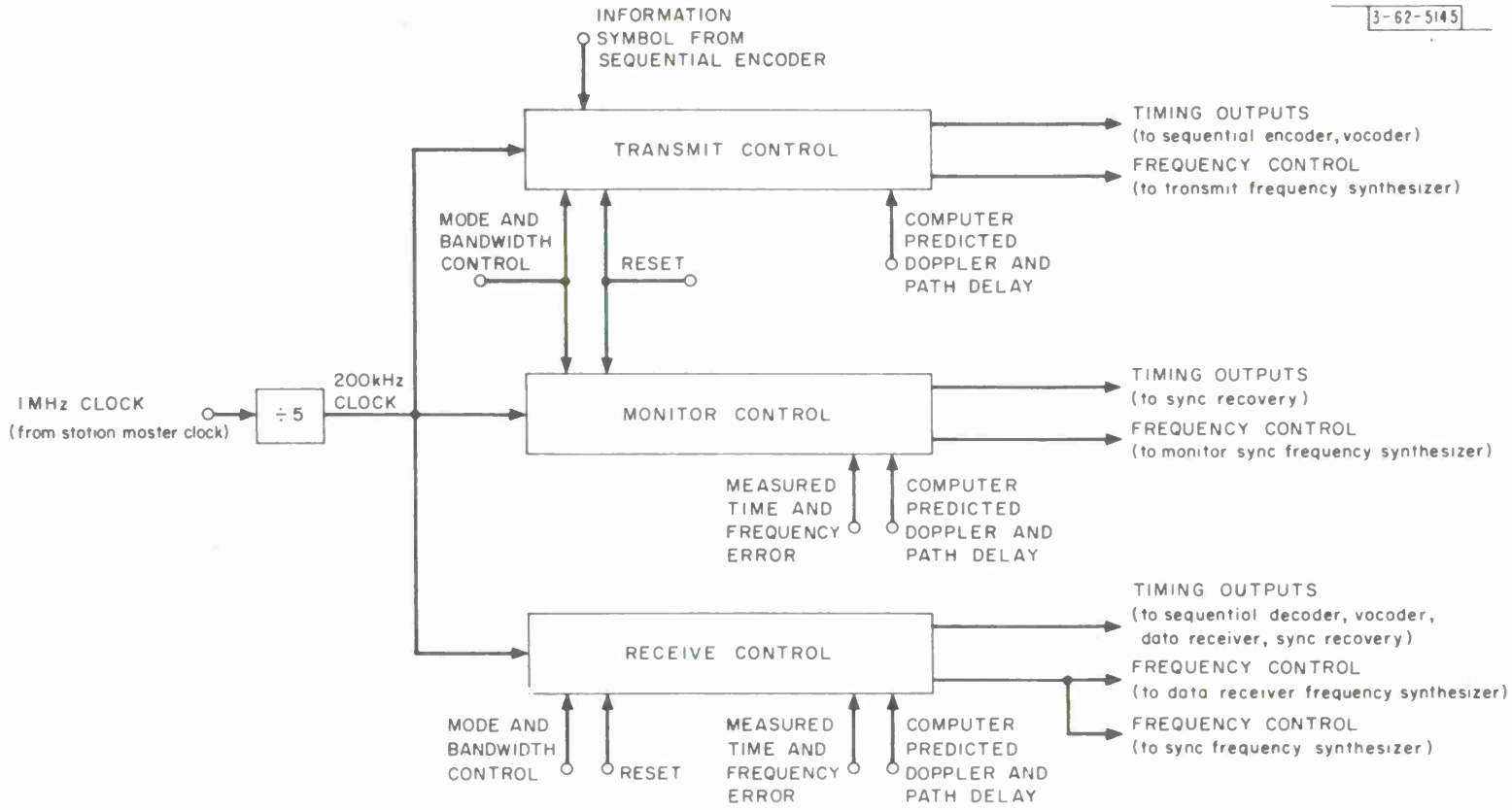

Fig. 1. Timing and frequency control.

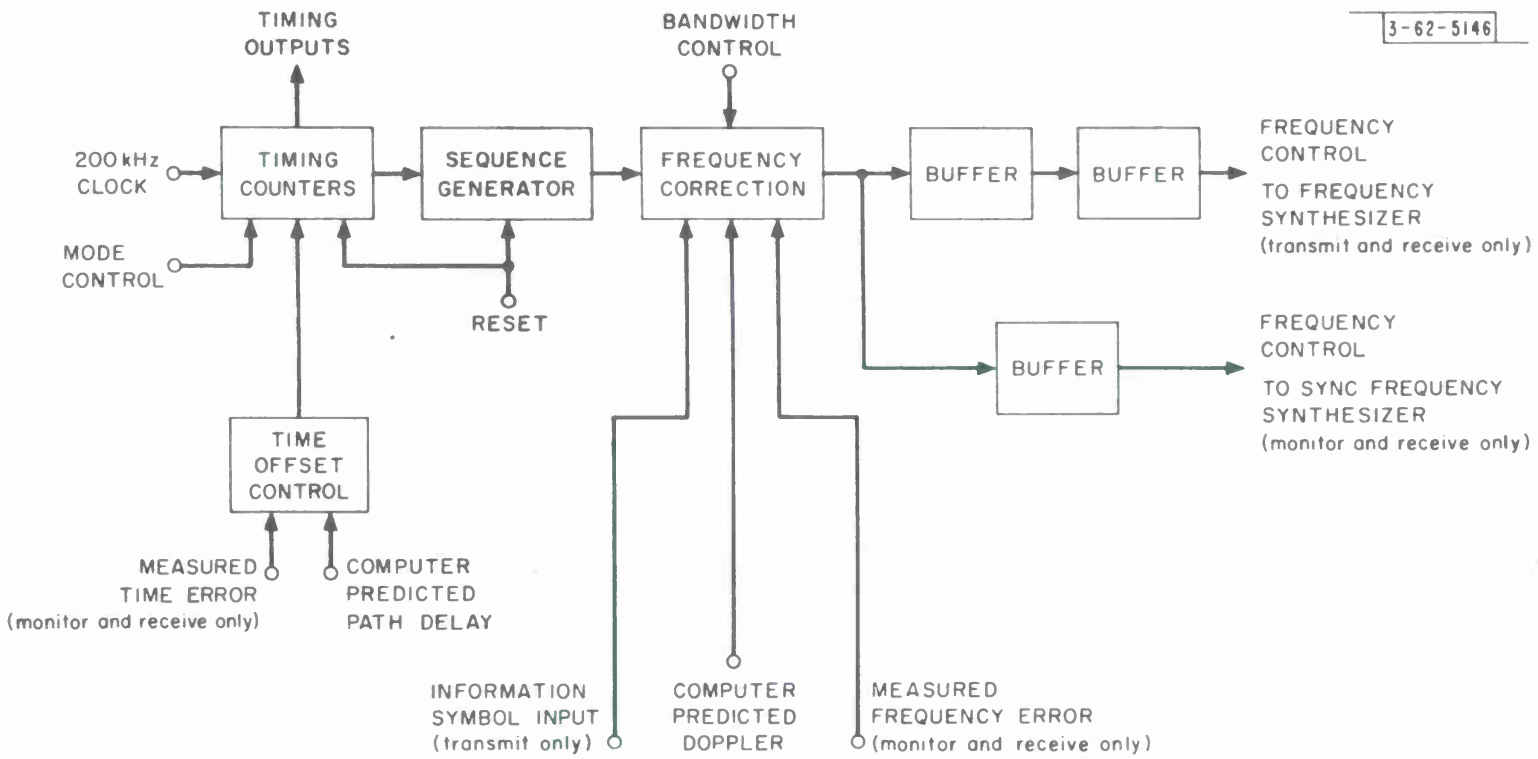

Fig. 2. Individual control section.

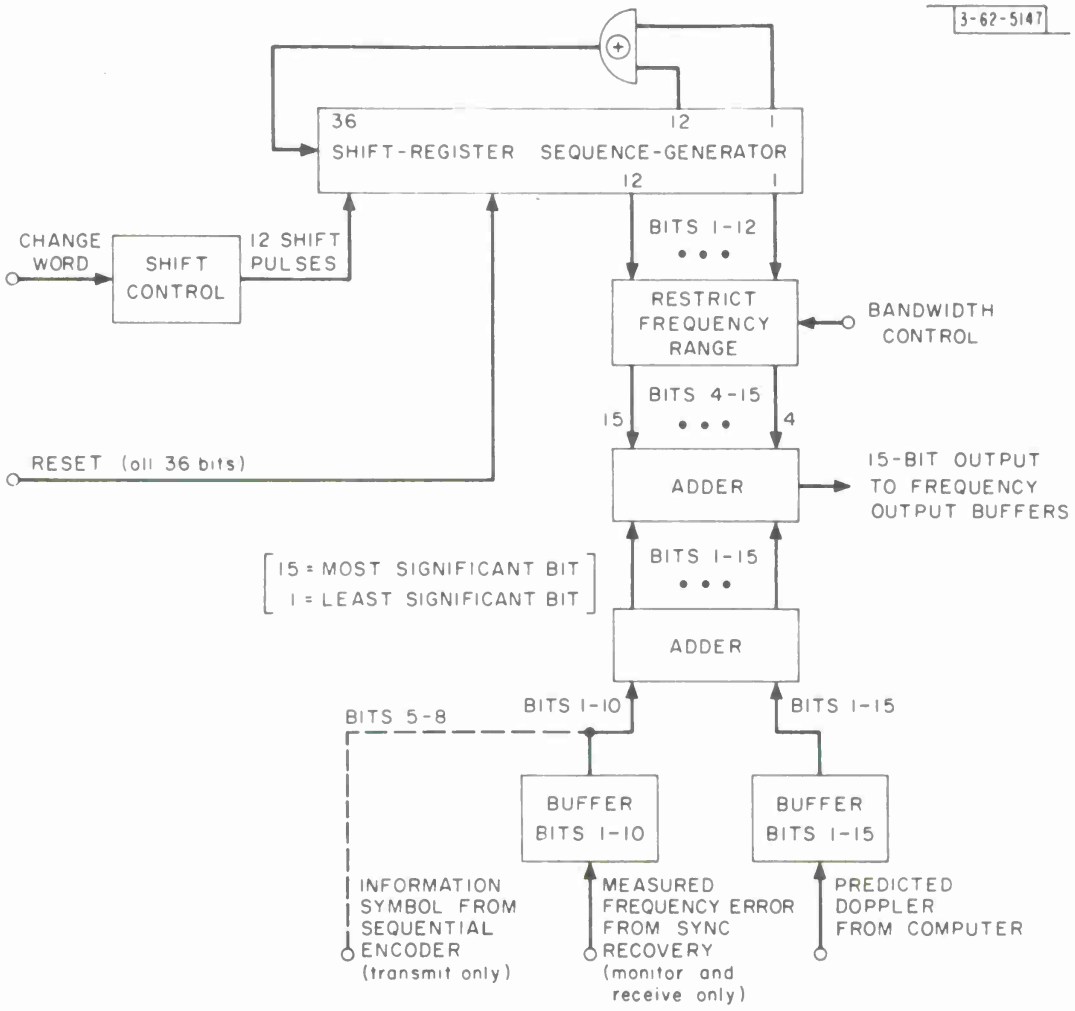

Fig. 3. Details of frequency control.

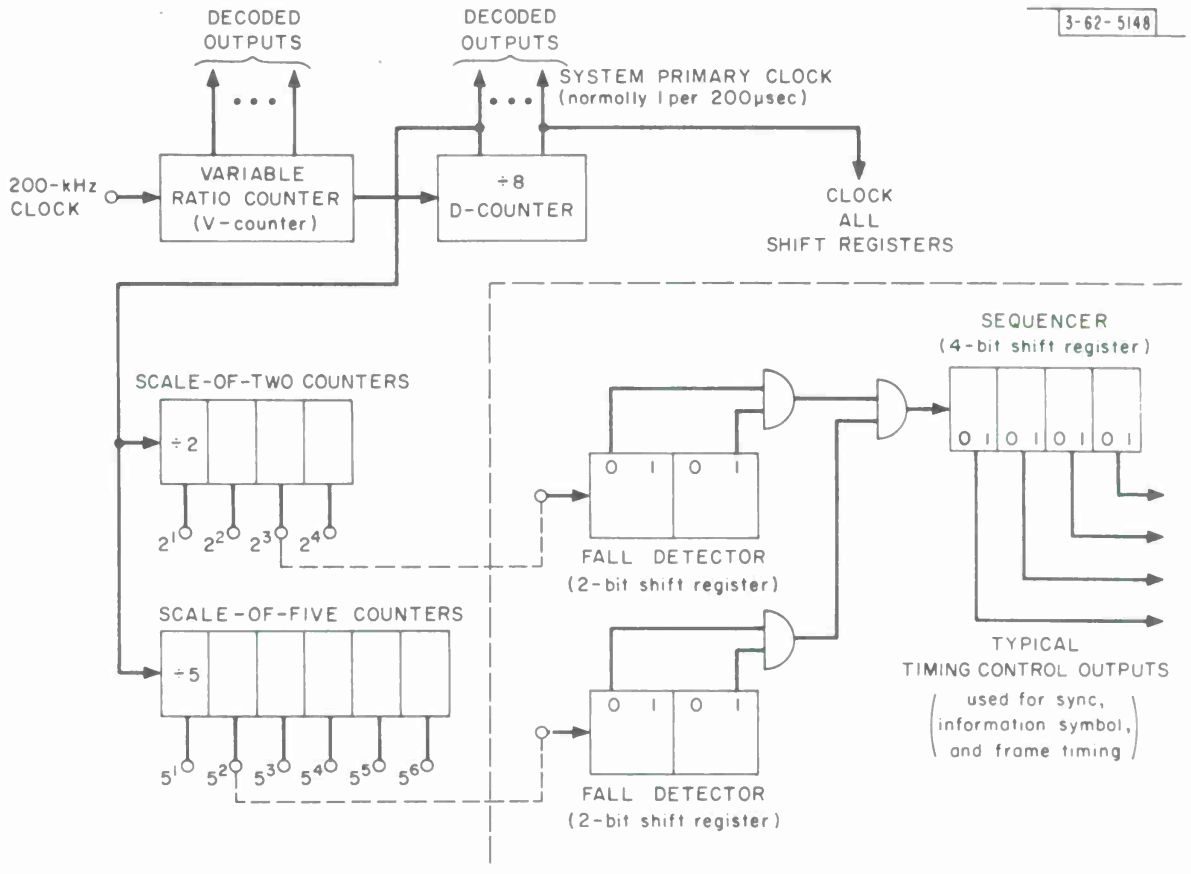

Fig. 4. Timing control logic.

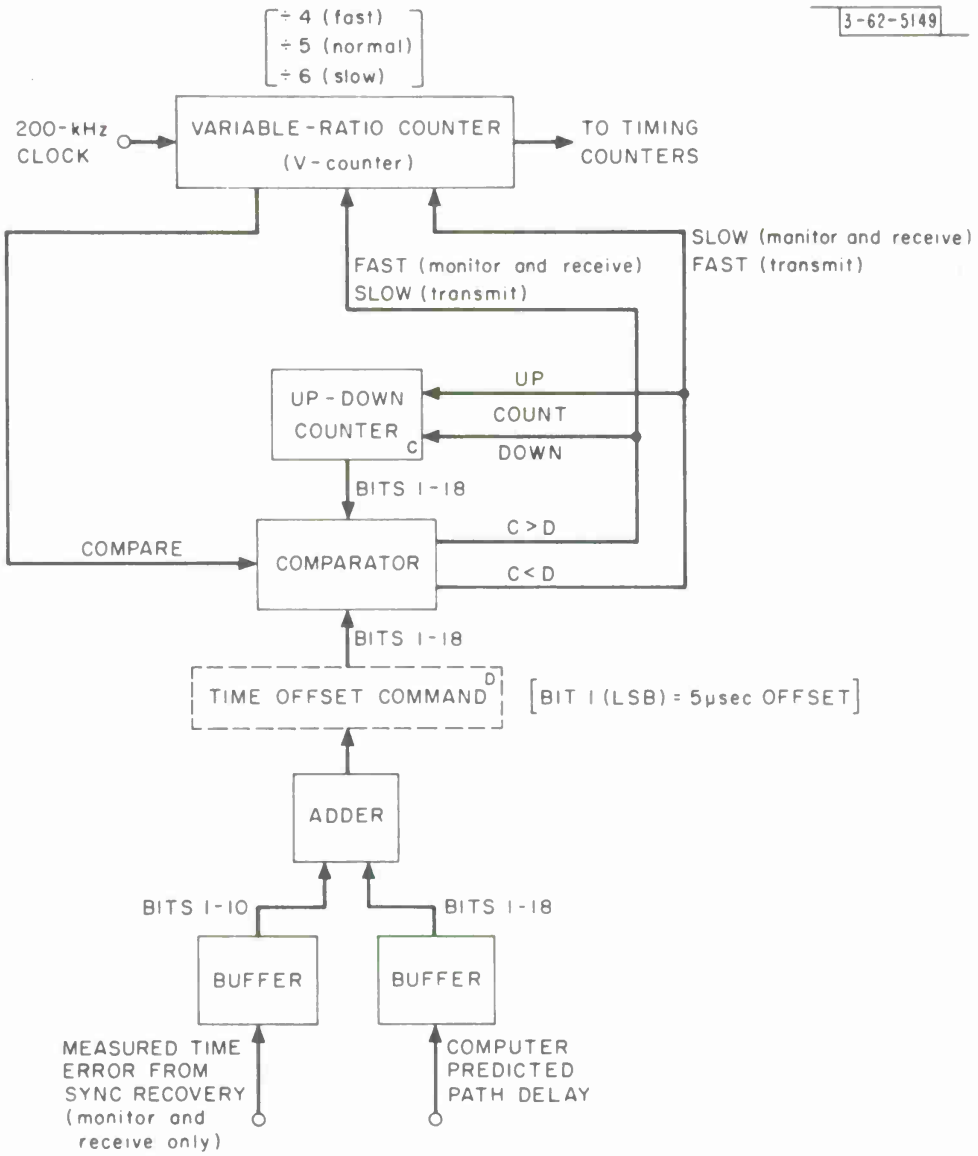

Fig. 5. Details of time offset control.

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(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY *(Corporate author)* Lincoln Laboratory, M. I. T.	2a. REPORT SECURITY CLASSIFICATION Unclassified 2b. GROUP None

3. REPORT TITLE

Lincoln Experimental Terminal Timing and Frequency Control

4. DESCRIPTIVE NOTES *(Type of report and inclusive dates)*

Technical Note

5. AUTHOR(S) *(Last name, first name, initial)*

Daggett, Norman L.

6. REPORT DATE	7a. TOTAL NO. OF PAGES	7b. NO. OF REFS
4 August 1966	18	2

8a. CONTRACT OR GRANT NO. AF 19(628)-5167 b. PROJECT NO. 649L c. d.	9a. ORIGINATOR'S REPORT NUMBER(S) Technical Note 1966-33 9b. OTHER REPORT NO(S) *(Any other numbers that may be assigned this report)* ESD-TR-66-399

10. AVAILABILITY/LIMITATION NOTICES

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11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY
None	Air Force Systems Command, USAF

13. ABSTRACT

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14. KEY WORDS

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timing
frequency control